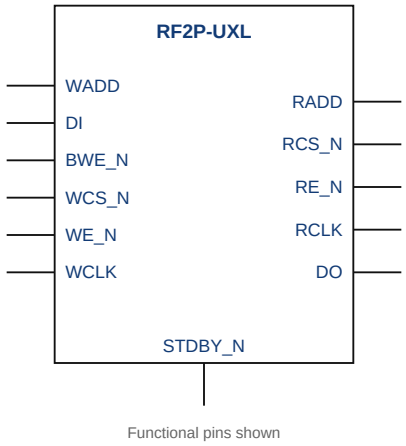
RF2P-UXL-GF22FDX-PLUS

Dual Port, Voltage Scaling

Register File Compiler

Dual-Port Architecture: Independent read-only and write-only ports support separate RCLK/WCLK, addresses, chip enables, and synchronous or asynchronous operation.
Voltage Scaling: Periphery VDD supports 0.5 V to 0.8 V nominal operation while the register-file array operates at 0.8 V (VDM); level translation is internal to the macro.
Low-Leakage Retention: Dedicated standby mode uses array source biasing and isolated array/periphery supplies so VDD can be powered off while memory contents are retained.
Bit Cell: Uses GLOBALFOUNDRIES 22FDX-PLUS 8T TP185SL bit cells with a drawn area of approximately 0.185 µm². Compiler enables "pre-charge" of bit line which reduces primary source of leakage in this bit cell.
Bit / Byte Write: Optional bit write enables independent writes to any subset of a word; programmable byte-wide write enable reduces control-pin count.
Error Protection: Optional SECDED logic provides single-bit correction and dual-bit detection, including support for multiple correctable units within a word.
Body Bias & Power Modes: Optional RBB control adjusts periphery speed/leakage. Five power states support fully on, periphery standby, full standby, retention, and power off.
Test & DFT Support: Optional soft BIST muxing, scan bypass, generic/Tessent ATPG views, and Tessent MBIST control simplify production test integration.



Functional pins shown

Technology	GF 22nm FDX-PLUS
Bit Cell	8T TP185SL, 0.185 µm²
Periphery VDD	0.5 - 0.8 V nominal
Array VDM	0.8 V nominal
Temperature	-40°C to +125°C
Power	Mesh
# Metal Layers	4
Modes	Functional / BIST / Scan / Sleep
Interface	Command line

Ports	1 read-only / 1 write-only
Max Instance	32 Kb
Min Instance	128 b
Word Width	4 - 64 bits
Word Depth	16 - 1024 words
Column Fold	4 / 8
Write Enable	Optional bit or byte
Error Correction	SECDED

EDA Views (Partial List)	
GDSII Layout	LEF
LVS SPICE Netlist	Liberty: NLDM / CCS / LVF
Behavioral Verilog + Testbench	Structural Verilog
UPF / CPF Power Models	ATPG: generic / Tessent
Tessent MBIST Control	PDF / Text Datasheets
Bitmap (x,y)	APL PWL Power Model
Voltus Power Grid Scripts	Hierarchical LVS cell list

About Nordic Semiconductor

Nordic Semiconductor's Seattle memory team provides SRAM, ROM, and Register File compilers optimized for ultra-low power, leakage, and high-performance applications.

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