SP-ULL-GF22FDX-PLUS

Single Port Low Leakage

SRAM Memory Compiler

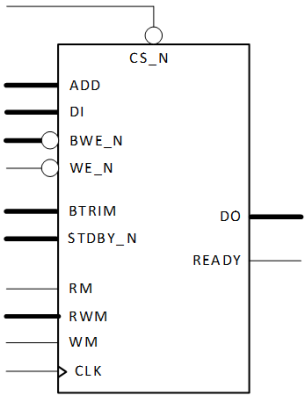
Ultra-Low Leakage: High V_T (HV_T) and low leakage ($LLHV_T$) devices are used with source biasing to minimize standby currents while operating at low voltage

Bit Cell: Utilizes GlobalFoundries® Ultra-Low Leakage 6T (P110UL) bit cells to ensure high manufacturing yields

Five Power Modes: High Performance, Low Leakage, Standby, Retention, and Power Off modes provide flexibility for power optimization

Speed Grades: Three options to adjust the speed/leakage balance and optimize for high speed or low power operation

Memory Ready Output: Create a Pseudo-Dual Port memory utilizing the READY pin



High-Density Solutions: Abutment capability to enable multi-instance macros

Data Write-Through: Optionally prevent data out transitions during a write to reduce power

Error Correction: Optional SECDED logic for single-bit correction and dual-bit detection

Technology	GF 22nm FDX **PLUS**	**Max Instance**	640 Kilobits	**EDA Views (Partial List)**	
Voltage	0.8V (typical)	**Min Instance**	256 Bits	Verilog Model with UPF	
Temperature	-40°C to +125°C	**Word Width**	4 – 144	Liberty Files (NLDM, LVF, CCS)	
Power	Mesh	**Banks**	1 or 2	PDF and Text Datasheets	Redhawk APL
# Metal Layers	4 (or 6 if 2 banks)	**Word Depth**	32 – 8192	LEF 5.8	Verilog Test Bench
Speeds	Slow | Medium | Fast	**Aspect Ratio**	Column Fold: 4, 8 or 16	LVS SPICE Netlist	Bitmap File (x, y)
BIST Mux	Internal	**Redundancy (CMFOLD 8, 16)**	Optional (4 or 8 repairs)	GDS	Power Grid (Voltus)
Modes	Functional, BIST, Scan, Sleep	**Write Enable**	Optional Bit or Byte	Tessent MBIST Control File	Common Power Format (CPF)

About Nordic Semiconductor

Nordic Semiconductor's Seattle memory team (formerly Mobile Semiconductor) provides SRAM, ROM, and Register File compilers optimized for ultra-low power, leakage, and high performance applications.

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