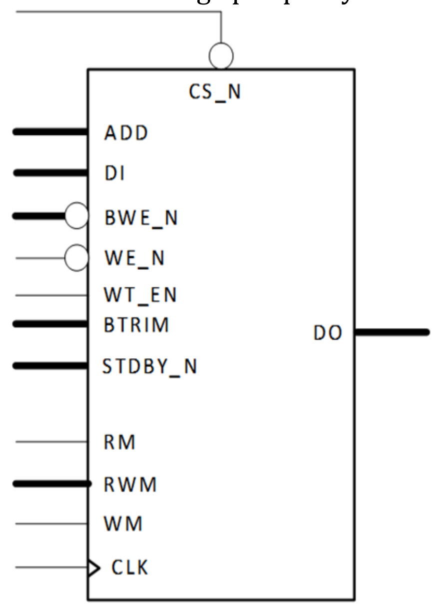
SP-HSB-GF22FDX-PLUS

Single Port High-Speed

Multi Bank SRAM Memory Compiler

Ultra-Low Leakage - GLOBALFOUNDRIES low-leakage 6T L110 bit cells with High Vt and low leakage periphery to ensure minimal leakage and high yield.



Multi-Bank Architecture - Memory split into 1 to 4 banks for reduced bit line length and enhanced timing.

Ultra Low Power Standby - Built-in source biasing trims standby current to a minimum for data retention.

Isolated Supplies - Independent periphery and array power domains allow periphery shutdown in standby.

Bit/Byte Write Enable - Selectively write individual bits or bytes within a word**.**

Write Through & Margin Controls - Pin-configurable write-through and read/write timing margin adjustments.

Error Correction - Optional SECDED logic for single-bit correction and dual-bit detection.

Technology & Specs

Technology	22FDX-PLUS
Voltage	0.65V*/0.8V (0.72V to 0.88V)
Temperature	-40°C to +125°C
Power	Mesh
# Metal Layers	4
BIST Mux	Internal
Modes	Functional, Sleep

***To be evaluated**

Max Instance	1.2 Mb
Min Instance	1 kb
Word Width	8 – 144
Word Depth	64-32768
Aspect Ratio	Column Fold: 4, 8, 16
User Interface	Command line
Bit Write Enable	Optional bit or byte

EDA Views (Partial List)	
Verilog Model with UPF	
Liberty Files (NLDM, LVF, CCS)	
PDF and Text Datasheets	Redhawk APL
LEF 5.8	Verilog Test Bench
LVS SPICE Netlist	Bitmap File (x, y)
GDS	Power Grid (Voltus)
Tessent MBIST Control File	Common Power Format (CPF)

About Nordic Semiconductor

Nordic Semiconductor's Seattle memory team (formerly Mobile Semiconductor) provides SRAM, ROM, and Register File compilers optimized for ultra-low power, leakage, and high-performance applications.

🔗 www.mobile-semiconductor.com

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