# SP-HSB-GF22FDX-PLUS



## **Single Port High-Speed**

### **Multi Bank SRAM Memory Compiler**

**Ultra-Low Leakage** - GLOBALFOUNDRIES low-leakage 6T L110HD bit cells ensure minimal leakage and high yield.

Multi-Bank Architecture - Memory split into 1 to 4 banks for reduced bit line length and enhanced timing.

**Ultra Low Power Standby** - Built-in source biasing trims standby current to a minimum for data retention.

**Isolated Supplies** - Independent periphery and array power domains allow periphery shutdown in standby.

**Bit/Byte Write** Enable - Selectively write individual bits or bytes within a word.

**Write Through & Margin Controls** - Pin-configurable write-through and read/write timing margin adjustments.

**Error Correction** - Optional SECDED logic for single-bit correction and dual-bit detection.

**Reverse Body Bias (Optional)-** Licensed option for body bias voltage control with custom timing/power characterization.

#### **Technology & Specs**

$\square$							
	CS_N						
	ADD						
	DI						
	BWE_N						
——C	WE_N						
	WT_EN BTRIM	DO					
	STDBY_N						
	RM						
	RWM						
	WM						
	> CLK						

Technology	22FDX-PLUS	Max Instance	1.2 Mb	EDA Views (Partial List)	
Voltage	0.8V (0.72V to 0.88V)	Min Instance	1 kb	Verilog Model with UPF	
Temperature	-40°C to +125°C	Word Width	8 – 144	Liberty Files (NLDM, LVF, CCS)	
Power	Mesh	Word Depth	64-32768	PDF and Text Datasheets	Redhawk APL
# Metal Layers	4	Aspect Ratio	Column Fold: 4, 8, 16	LEF 5.8	Verilog Test Bench
BIST Mux	Internal	User Interface	Command line	LVS SPICE Netlist	Bitmap File (x, y)
Modes	Functional, Sleep	Bit Write Enable	Optional bit or byte	GDS	Power Grid (Voltus)
				Tessent MBIST Control File	Common Power Format (CPF)

#### **About Mobile Semiconductor**

Nordic Semiconductor's Seattle memory team (formerly Mobile Semiconductor) provides SRAM, ROM, and Register File compilers optimized for ultra-low power, leakage, and high-performance applications.

 $\diamond$  www.mobile-semiconductor.com

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