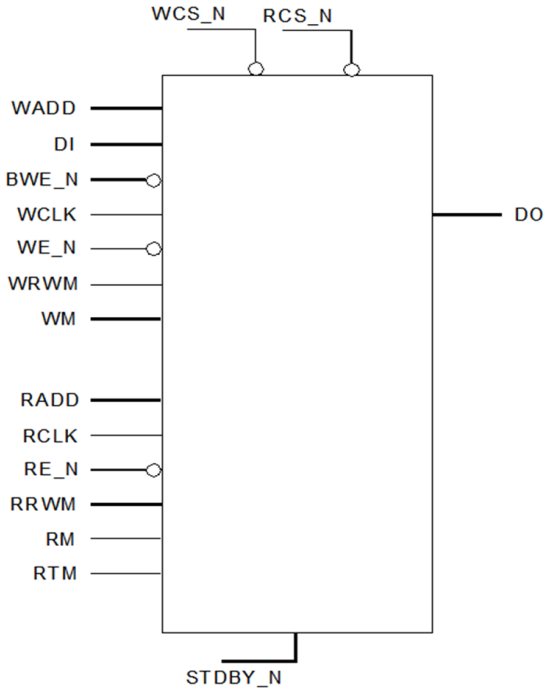
RF2P-ULS-GF22FDX-PLUS

Dual Port Register File Compiler

(1 Read-only port, 1 Write-only port)



Highlights

- Low Leakage: Uses modified 8T-TP185SL bit cells with high V_T read port for reduced leakage and larger instance support.
- Isolated Supplies: Periphery and array power domains can be independently powered down in standby mode.
- Deep Sleep Standby Mode: Memory retains data at minimal power via internal biasing.
- Timing Margin Controls: Internal pins adjust read/write timing margins.
- Integrated BIST Mux Integration for Built-In Self Test support.
- Speed vs Leakage Tradeoff Option

Technology and Specs

Technology	22FDX-PLUS	**Max Instance**	64 Kb
Voltage	0.8V (0.72V to 0.88V)	**Min Instance**	128b
Temperature	-40°C to +125°C	**Word Width**	4-64
Power	Mesh	**Word Depth**	16-2048
# Metal Layers	4	**Aspect Ratio**	Column Fold: 4 or 8
BIST Mux	Internal	**User Interface**	Command line
Modes	Functional, Sleep, Bist, Scan	**Bit Write Enable**	Optional

EDA Views (Partial List)	
Verilog Model with UPF	
Liberty Files (NLDM, LVF, CCS)	
PDF and Text Datasheets	Redhawk APL
LEF 5.8	Verilog Test Bench
LVS SPICE Netlist	Bitmap File (x, y)
GDS	Power Grid (Voltus)
Tessent MBIST Control File	Common Power Format (CPF)

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