

RF2P-ULL-GF22FDX-PLUS

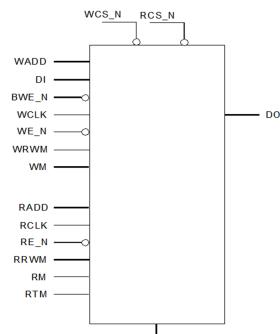
Dual Port Register File Compiler

(1 Read-only port, 1 Write-only port)

Highlights

- Uses 8T-TP185SL bit cells.
- Isolated Supplies: Periphery and array power domains can be independently powered down in standby mode.
- Deep Sleep Standby Mode: Memory retains data at minimal power via internal biasing.
- Timing Margin Controls: Internal pins separately adjust read and write timing margins.
- Integrated BIST Mux for Built-In Self Test support.
- Speed vs Leakage Tradeoff Option

Technology & Specs



STDBY_N

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Technology	22FDX-PLUS	Max Instance	32Kb	EDA Views (Partial List)	
Voltage	0.8V (0.72V to 0.88V)	Min Instance	128b	Verilog Model with UPF	
Temperature	-40°C to +125°C	Word Width	4-64	Liberty Files (NLDM, LVF, CCS)	
Power	Mesh	Word Depth	16-1024	PDF and Text Datasheets	Redhawk APL
# Metal Layers	4	Aspect Ratio	Column Fold: 4 or 8	LEF 5.8	Verilog Test Bench
BIST Mux	Internal	User Interface	Command line	LVS SPICE Netlist	Bitmap File (x, y)
Modes	Functional, BIST, Scan, Sleep	Bit Write Enable	Optional	GDS	Power Grid (Voltus)
				Tessent MBIST Control File	Common Power Format (CPF)

About Mobile Semiconductor

Nordic Semiconductor's Seattle memory team (formerly Mobile Semiconductor) provides SRAM, ROM, and Register File compilers optimized for ultra-low power, leakage, and high-performance applications.

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