

SP-LVR-TS22ULL



Single Port Low Voltage

SRAM Memory Compiler

Low Power Retention and Column Repair

Ultra-Low Leakage: High V_T (HV_T) are used to minimize leakage performance

Bit Cell: Utilizes Low Leakage 6T bit cells to ensure high manufacturing yields

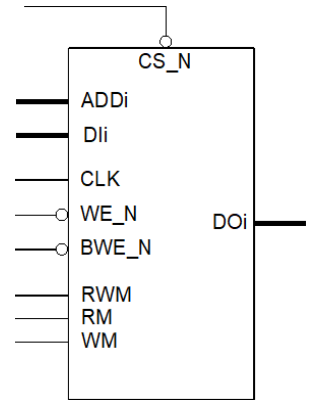
Ultra Low Power Standby: Internally generated bias voltage for low leakage data retention

Isolated Array and Periphery supplies: Periphery voltage can be shut off to further reduce standby power

Data Write-Through: Pin controllable write through disables data out transitions during a write to reduce power. During ATPG data out is controllable to ensure for full coverage

Error Correction: Single bit error correction and dual bit error detection (SECDED) is optionally included in the synthesizable wrapper.

Column Repair: Has 4 repairable elements



Technology	CLN22ULL	Max Instance	256Kb	EDA Views (Partial List)	
Voltage	0.9V (0.81V to 0.99V)	Min Instance	512 Bits	Verilog Model with UPF	
Temperature	-40°C to +125°C	Word Width	8 – 1128	Liberty Files (NLDM, LVF, CCS)	
Power	Mesh	Word Depth	32 – 4096	PDF and Text Datasheets	Redhawk APL
# Metal Layers	4	Aspect Ratio	Column Fold: 4 or 8	LEF 5.8	Verilog Test Bench
BIST Mux	Internal	User Interface	Command line	LVS SPICE Netlist	Bitmap File (x, y)
Modes	Functional, BIST, Scan, Sleep	Bit Write Enable	Optional	GDS	Power Grid (Votus)
				Tessent MBIST Control File	Common Power Format (CPF)

About Mobile Semiconductor:

Nordic Semiconductor's Seattle, Washington memory team continues building on the technology acquired from Mobile Semiconductor. SRAM, ROM, and Register File compilers are available for applications requiring ultra-low power, low leakage, or ultra-high performance.

<http://www.mobile-semiconductor.com/>

© September 2024 Nordic Semiconductor All rights reserved