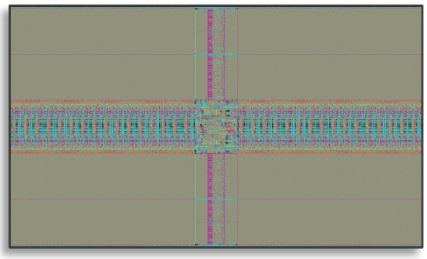
Committed to Memory

SP-HSLV-TS40ULPF High Speed Single Port Compiler

Low voltage. Mobile Semiconductor's SP-HSLV-TS40ULPF memory compiler generates single-port SRAM instances using the TSMC 40nm ULP CMOS process. Each low voltage memory instance uses standard V_T to optimize performance with high V_T and source biasing to minimize standby currents. Read and write assist circuits ensure reliable operation with a power supply as low as 0.72V.



Ultra low power data retention. Memory instances generated by the SP-HSLV-TS40ULPF go into a deep sleep mode that retains data at minimal power consumption.

Self biasing. The SP-HSLV-TS40ULPF's internal self-biasing capabilities provide ease of IP integration.

Soft error immunity. Robust, low voltage latches are used throughout designs.

High yield. To ensure high manufacturing yield, the SP-HSLV-TS40ULPF utilizes TSMC's high V_T 6T ($0.242\mu^2$) bit cells and is consistent with TSMC's Design for Manufacturing (DFM) guidelines for the 40nm ULP process.

High usability. All signal and power pins are available on metal 4 while maintaining routing porosity in metal 4.

Memory Compiler EDA Views & Outputs
GDS II Layout
LVS SPICE Netlist
Liberty File (NLDM and CCS)
Verilog Model
Verilog Netlist
Verilog RTL Wrapper
Verilog Test Bench
ATPG Verilog
LEF
BIST Synthesis Control File
Signal Integrity Analysis Models
PDF and Text Datasheets

Process Technology	TSMC 40nm ULP
Supply Voltage	0.72V to 1.21V
Operating Temperature	-40°C to +125°C
Operating Frequency	200MHz to 500MHz
# Metal Layers	4
Power	Mesh
BIST Mux Interface	Internal
Operational Modes	Functional, BIST and Scan

Max Instance	512Kb
Min Instance	256b
Word Width	4–128
Word Depth	64–8192
Aspect Ratio	Column Fold, 8 or 16
Bit Write Enable	Optional
User Interface	GUI & Command Line

www.mobile-semi.com
embedded-solutions@mobile-semi.com

209 1/2 First Ave South
Suite 300
Seattle, WA 98104
Phone: 408 461 7726
Fax: 206.971.7439