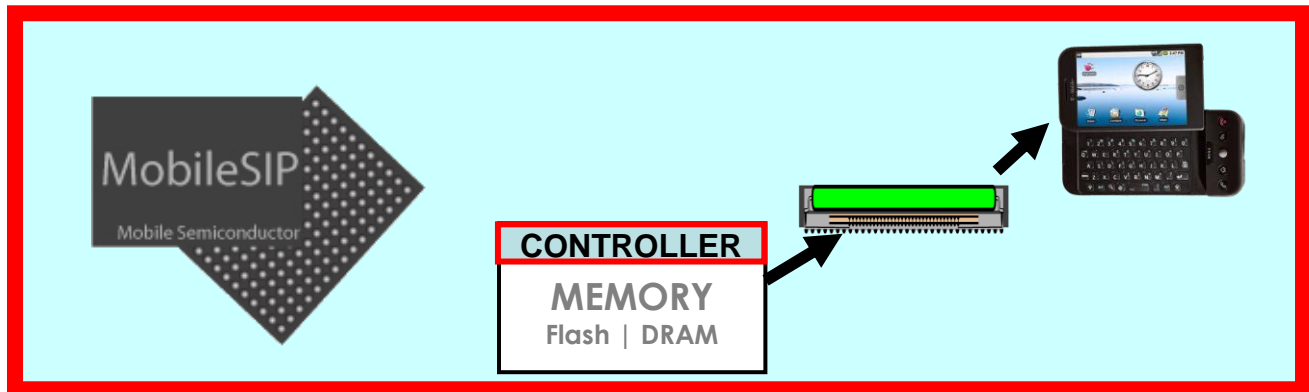


## Product Brief

### Smartphone Memory System

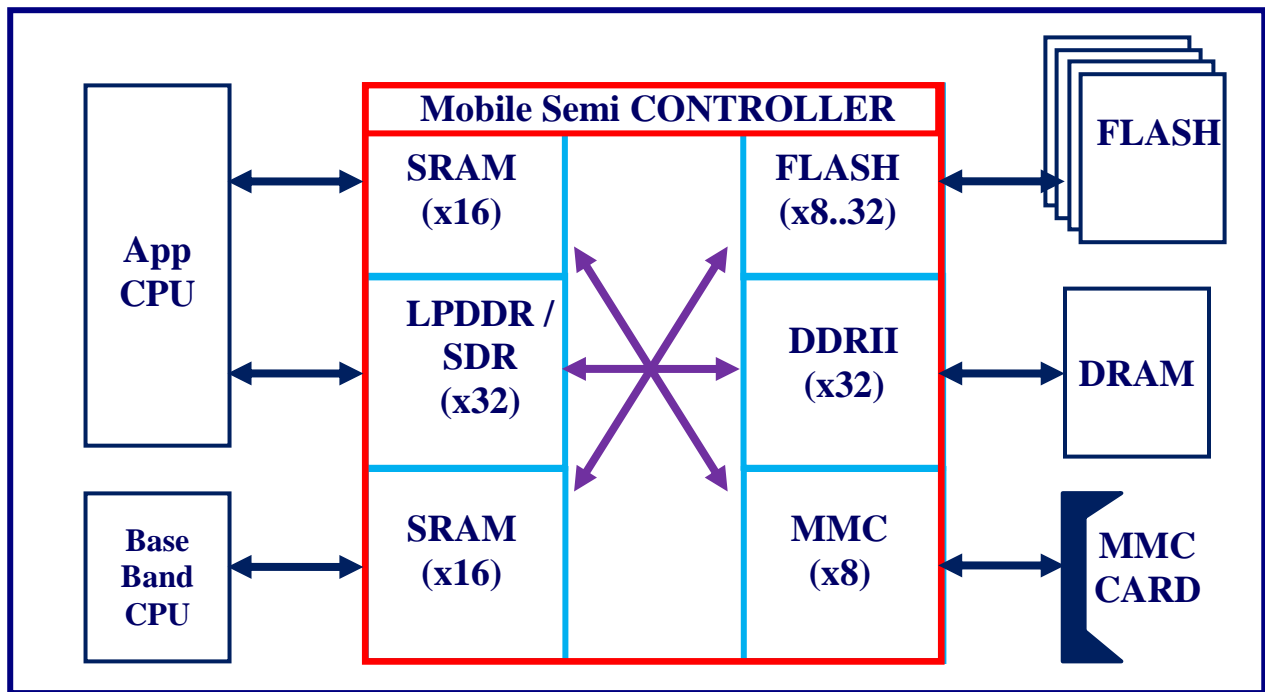


Mobile Semiconductor's memory system architecture is designed for advanced mobile handsets (smartphones) and 3G or 4G video broadcast devices. Our technology can improve a variety of mobile computing devices such as game players, advanced MP3 players, or mobile video players.

**This product brief describes the capabilities of the MobileSIP memory controller. For detailed application information, please contact Mobile Semiconductor Corporation.**

#### Features:

- Advanced architecture controller combined with Mobile DRAM and NAND Flash
- A complete memory solution for the handset
- From 1 to 16GigaBytes SLC or MLC NAND Flash
- From 64 to 256 Mega Bytes SDR or DDR DRAM
- Burst read: 830 Mega Bytes/sec, Sustained read: over 100 MB/sec
- Embedded Flash File System for easy integration with OS
- SRAM interface provides Bootable Partitions
- JEDEC 79-4 LPDDR interface for maximum performance
- Built in MMC interface for maximum performance expansion memory.
- Auxiliary SRAM port for dual core access to the memory
- Power saving architecture
- Proprietary caching mechanisms to reduce application load times and memory footprint



**Figure 1 Controller Interface Ports**

MobileSIP is a high speed memory system, combining NAND FLASH, Mobile DDR DRAM, and a memory controller in a single multi chip package.

MobileSIP provides a substantial performance advantage for application processing in mobile devices including smartphones, Mobile Internet Devices (MID), and ultra mobile PCs (UMPC).

A 16 bit SRAM style interface provides up to 128 kBytes for processor boot.

The physical interface for the application processor to the Mobile DDR is through a JEDEC LPDDR standard mobile DRAM interface.

Operating system interface to both the embedded NAND storage and the MMC port is at the file system level, using an installable file system (IFS). The file system is accessed by the driver by a series of commands written into memory map registers. These registers are accessible through either the SRAM interface or through the LPDDR interface.

The MMC port allows for expansion storage capacity that may be seamlessly integrated into the same file system as the onboard storage capacity. Expansion storage is typically mounted as a distinct volume in the file system.

Auxiliary 16 bit SRAM interface may be configured to boot a second processor (baseband), and to facilitate communication between the two processors.

The sector based file system is compatible with multiple file systems including FAT and FAT32. For optimum performance and reliability, use of the transactional based file system, Datalight Reliance™ is recommended.

