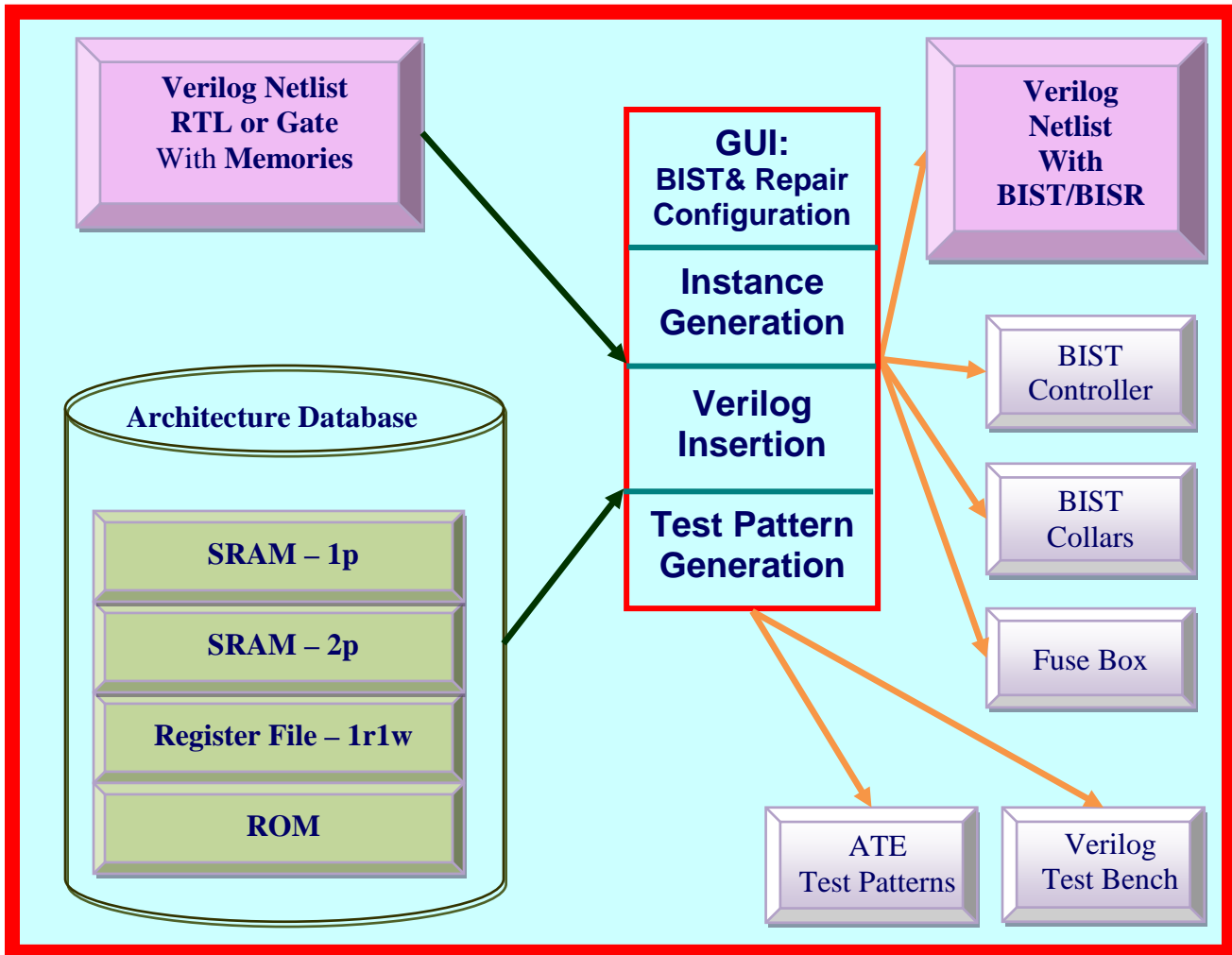


Product Brief

EMS² Test & Repair (T&R) for Embedded Memories



EMS² T&R is a complete memory test and repair solution that interfaces with multiple third party BIST solutions*. Features and capabilities of this system have been optimized to insure efficient and complete test coverage and optimal yield of embedded memories in advanced process technologies.

Features:

- Supports single port SRAM, dual port SRAM, register file, and ROM instances
- At-Speed Built in Self Test capability (BIST)
- Built in Self Repair (BISR)
- Integrated fuse box
- IEEE 1149.1 interface
- Test bench generation
- Automated insertion of self test logic into existing verilog netlist

* Requires third party BIST software license

EMS² T&R is a fully automated memory test and repair generator. It maintains a project level instance database, for ease of partitioning and allowing generation of unified test vectors for Automatic Test Equipment (ATE).

Following are only some of highlights of TrailBlaze™ BISTAR

- Automatically Locates memory instances in the netlist and provides an initial partitioning of instances into groups for shared BIST controller
- GUI-driven to simplify tool usage and provide feedback of area cost and yield
 - Select memory instances to share a BIST controller
 - Allows parallel test with multiple BIST controllers, analyzing impact on test time and power
 - Select BIST controllers to share FUSE box: maximize yield at minimum area impact

❖ Output Views:

- **Verilog: RTL or gate level after BIST insertion**
- **PDF Datasheet**
- **System Verilog test bench**
- **Test patterns for ATE**
- **RTL for BIST controllers and BIST collars as required**
- **Synthesis scripts**
- **Fuse box:**
 - **PDF Datasheet**
 - **Verilog behavioral model**
 - **GDS Full layout**
 - **GDS P&R Abstract with signal, power and blockage information**
 - **Liberty File with current mode timing, static and active power, noise models**
 - **LEF version 5.6**
 - **Setup files to generate Apollo FRAM P&R view**
 - **SPICE netlist for LVS**
 - **List of cells for hierarchical LVS (also auto-match compliant)**