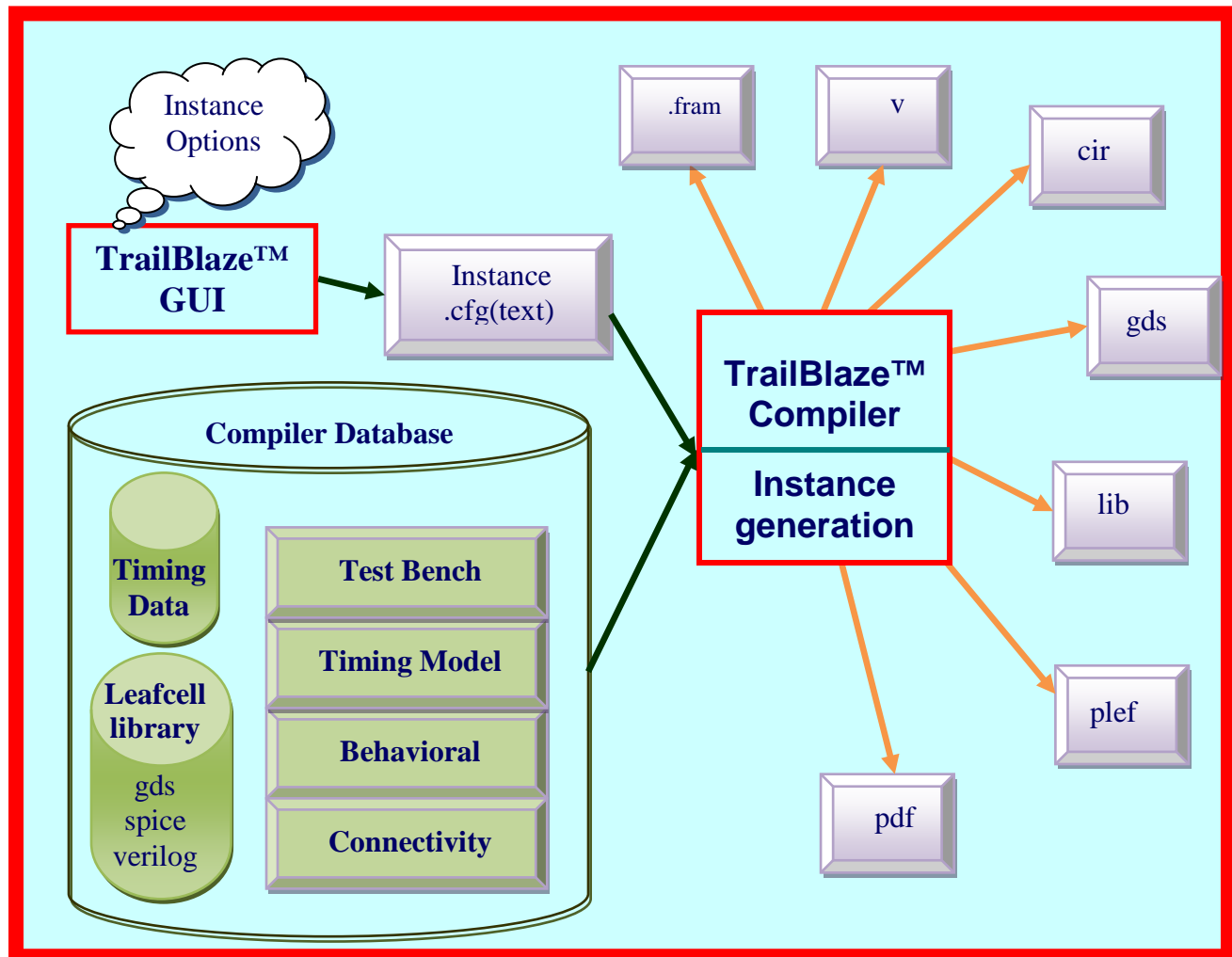


Product Brief

EMS² TrailBlaze™ – Custom Developed Embedded Memory Compilers



Mobile Semiconductor has an extensive experience in developing an array of custom design embedded SRAMs and memory compilers that are fully functional and error-free at first pass.

Our compilers will be custom developed based on specific needs or market segment requirements. Compiler can target any applications requiring following features:

- Ultra High Speed
- Ultra High Density
- Ultra Low Power

This product brief describes the capabilities of the TrailBlaze custom compiler that generates instances developed for variety of different processes or technologies.

For more information on specific memory configurations (SP, DP, MP), please refer to each individual product briefs.

Following are only some of highlights of TrailBlaze™ compiler:

- Complete memory instance generation in minutes
- GUI-driven to simplify tool usage
- Range checking of user options to insure valid instance configuration
- Estimation of timing, power & area based on user instance size to allow quick evaluation of options
- Text configuration file for command line operation and easy CAD flow integration
- Physical views compliant to Cadence, Synopsys, Magma, Mentor tools
- Voltage Scaling compliant timing models
- Built in interpolation and de-rating capability.
- Standard BIST tool compatibility
 - Mentor-MBIST;
 - Synopsys-DesignWare Memory BIST
- Built in capability to re-characterize to new operating conditions or models at any time
 - All or partial data collection (for example standby power, but no timing)
 - Does not require any third-party licenses

TrailBlaze™ is a fully automated memory instance generator. It maintains a common instance database, which insures consistency between output views and allows for crosschecking to insure the utmost integrity in the output views.

❖ Output Views:

- PDF Datasheet
- Text based instance summary
- GDS layout: Power pins connect to upper metal; all pins on routing grid
- GDS P&R Abstract with signal, power and blockage information
- Liberty File with current mode timing, static and active power, noise models
- LEF version 5.6
- Setup files to generate Apollo FRAM P&R view
- SPICE netlist for LVS
- List of cells for hierarchical LVS (also auto-match compliant)
- Behavioral Verilog (with preload, fault modeling, fast models for running extensive vector sets, etc)
- Behavioral Verilog Test Bench
- Structural Verilog with test bench



Figure 1. Example of GUI